

Amendments to the Claims

1-4. (Canceled)

5. (Previously Presented) A circuit, comprising:

- a first delay line to delay a clock signal by a first amount of time;
- a second delay line to delay the clock signal by a second amount of time;
- a signal processor to generate a timing signal from the clock signal, the timing signal having a first edge controlled by the delayed clock signal generated by the first delay line and a second edge controlled by the delayed clock signal generated by the second delay line, wherein the signal processor includes:
 - a control circuit to generate an interim timing signal from the clock signal, the interim timing signal having edge transitions which coincide with one of a falling edge and a rising edge of the clock signal; and
 - a timing circuit to generate the timing signal from the interim timing signal, and

wherein the interim timing signal has a period which is substantially twice as long as the period of the clock signal.

6. (Previously Presented) The circuit of claim 5, wherein the timing circuit sets the first edge of the timing signal based on an edge transition of the delayed clock signal generated by the first delay line, and sets the second edge of the timing signal based on an edge transition of the delayed clock signal generated by the second delay line.

7. (Original) The circuit of claim 6, wherein the first edge of the timing signal corresponds to a logical value of the interim timing signal that exists at the time of the edge transition of the delayed clock signal generated by the first delay line, and wherein the second edge of the timing signal corresponds to a logical value of the interim timing signal that exists at the time of the edge transition of the delayed clock signal generated by the second delay line.

8. (Original) The circuit of claim 7, wherein the converter further includes:
a first logical transfer circuit to store said logical values of the interim timing signal prior to respective edge transitions of the delayed clock signals generated by the first and second delay lines, said first logical transfer circuit introducing delay that contributes to setting of the first and second edges of the timing signal.

9. (Original) The circuit of claim 8, further comprising:
a second logical transfer circuit to output the timing signal based on said logical values stored in the first logical transfer circuit.

10. (Original) The circuit of claim 9, wherein the first logical transfer circuit includes a latch and the second logical transfer circuit includes a flip-flop.

11. (Canceled)

12. (Previously Presented) A signal processing method, comprising:
delaying a clock signal by a first amount to form a first delayed clock signal;
delaying the clock signal by a second amount to form a second delayed clock

signal; and

generating a timing signal from the clock signal, the timing signal having a first edge controlled by the first delayed clock signal and a second edge controlled by the second delayed clock signal, wherein generating includes:

forming an interim timing signal from the clock signal, the interim timing signal having edge transitions which coincide with one of a falling edge and a rising edge of the clock signal; and

generating the timing signal from the interim timing signal, wherein the interim timing signal is periodic with a period which is substantially twice as long as the period of the clock signal.

13. (Original) The method of claim 12, wherein the timing signal assumes different logical values over a predetermined time period.

14. (Original) The method of claim 13, wherein the timing signal assumes a first logical value for a longer duration than a second logical value over the time period.

15-16 (Canceled)

17. (Previously Presented) The method of claim 12, wherein generating the timing signal includes:

setting the first edge of the timing signal based on an edge transition of the first delayed clock signal; and

setting the second edge of the timing signal based on an edge transition of the second delayed clock signal.

18. (Original) The method of claim 17, wherein the first edge of the timing signal corresponds to a logical value of the interim timing signal that exists at the time of the edge transition of the first delayed clock signal, and wherein the second edge of the timing signal corresponds to a logical value of the interim timing signal that exists at the time of the edge transition of the second delayed clock signal.

19. (Original) The method of claim 18, further comprising:
storing said logical values of the interim timing signal in a latch prior to respective edge transitions of the first and second delayed clock signals, said storing introducing delay that contributes to setting of the first and second edges of the timing signal.

20. (Original) The method of claim 12, further comprising:
changing at least one of the first and second amounts of delay to adjust a position of at least a corresponding one of the first and second edges of the timing signal.

21. (Previously Presented) A circuit, comprising:
a switch; and
a timing circuit to control input of a voltage signal through the switch, said timing circuit including:
a first delay line to delay a clock signal by a first amount of time,

a second delay line to delay the clock signal by a second amount of time, and
a signal processor to generate a timing signal from the clock signal, the timing signal having a first edge controlled by the delayed clock signal generated by the first delay line and a second edge controlled by the delayed clock signal generated by the second delay line, wherein different portions of the timing signal independently control input of the voltage signal through the switch.

22. (Previously Presented) The circuit of claim 21, wherein a first portion of the timing signal assumes a first logical value for a first period of time and a second portion of the timing signal assumes a second logical value for a second period of time different from the first period of time, and wherein the first logical value of the timing signal controls input of the voltage signal through the switch for the first period of time and the second logical value of the timing signal places the switch in an open position for the second period of time.

23. (Previously Presented) The circuit of claim 22, wherein the circuit is a converter which includes an LC circuit coupled to the switch, and wherein a DC level of the voltage signal is converted into a different DC level based on control of the switch by the timing signal.

24. (Original) A method, comprising:
delaying a clock signal by a first amount to form a first delayed clock signal;
delaying the clock signal by a second amount to form a second delayed clock signal;

generating a timing signal from the clock signal, the timing signal having a first edge controlled by the first delayed clock signal and a second edge controlled by the second delayed clock signal; and

controlling input of a voltage signal into a level converter based on the timing signal, wherein different portions of the timing signal independently control switching of the voltage signal into the level converter.

25. (Original) The method of claim 24, wherein a first portion of the timing signal assumes a first logical value for a first period of time and a second portion of the timing signal assumes a second logical value for a second period of time different from the first period of time.

26. (Original) The method of claim 25, wherein controlling input of the voltage signal includes:

connecting the voltage signal to the level converter through a switch for the first period of time based on the first logical value of the timing signal; and

placing the switch in an open position for the second period of time based on the second logical value of the timing signal.

27. (Original) The method of claim 24, wherein the level converter converts a DC level of the voltage signal into a different DC level.

28-30 (Canceled)

31. (Currently Amended) A circuit, comprising:

- a first delay line to delay a clock signal by a first amount of time;
- a second delay line to delay the clock signal by a second amount of time; and
- a signal processor to generate:
 - a) a first timing signal from the clock signal,
 - b) a second timing signal having edge transitions controlled by the first timing signal at times determined by a logical combination of the delayed clock signals from the first and second delay lines, and
 - c) a third timing signal having edge transitions controlled by the second timing signal at times determined by one of the delayed clock signals from the first and second delay lines, wherein the first timing signal has a period which is a number of times longer than the clock signal.

32. (Canceled)

33. (Currently Amended) The circuit of claim 31 ~~[[32]]~~, wherein said number is at least substantially two.

34. (Previously Presented) The circuit of claim 31, wherein the signal processor includes:

- a first logical circuit to control the edge transitions of the second timing signal based on logical values of the first timing signal at times determined by a logical combination of the delayed clock signals.

35. (Previously Presented) The circuit of claim 34, wherein the first logical circuit controls the edge transitions of the second timing signal based on logical values of the first timing signal at times when the delayed clock signals have a same logical value.

36. (Currently Amended) A [[The]] circuit of claim 34, comprising:
a first delay line to delay a clock signal by a first amount of time;
a second delay line to delay the clock signal by a second amount of time; and
a signal processor to generate:
a) a first timing signal from the clock signal,
b) a second timing signal having edge transitions controlled by the first timing signal at times determined by a logical combination of the delayed clock signals from the first and second delay lines, and
c) a third timing signal having edge transitions controlled by the second timing signal at times determined by one of the delayed clock signals from the first and second delay lines, wherein the signal processor includes:
a first logical circuit to control the edge transitions of the second timing signal based on logical values of the first timing signal at times determined by a logical combination of the delayed clock signals, wherein the first logical circuit includes a data input coupled to receive the first timing signal and a clock input coupled to receive a signal indicative of a logical combination of the delayed clock signals.

37. (Previously Presented) The circuit of claim 34, wherein the signal processor further includes:

a second logical circuit to control the edge transitions of the third timing signal based on logical values of the second timing signal at times determined by one of the delayed clock signals from the first and second delay lines.

38. (Previously Presented) The circuit of claim 37, wherein a different one of the delayed clock signals determines when the second logical circuit controls the edge transitions of the third timing signal at different times.

39. (Previously Presented) The circuit of claim 37, wherein the second timing signal determines which one of the delayed clock signals controls when the second logical circuit sets the edge transitions of the third timing signal based on logical values of the second timing signal.

40. (Previously Presented) The circuit of claim 37, wherein the second logical circuit includes a data input coupled to receive the second timing signal and a clock input coupled to a multiplexer, the multiplexer selecting for output one of the delayed clock signals based on a logical value of the second timing signal.

41. (Currently Amended) A ~~[[The]]~~ circuit of ~~claim 31, further~~ comprising:

a first delay line to delay a clock signal by a first amount of time;

a second delay line to delay the clock signal by a second amount of time;

a signal processor to generate:

a) a first timing signal from the clock signal,

b) a second timing signal having edge transitions controlled by the first timing signal at times determined by a logical combination of the delayed clock signals from the first and second delay lines, and

c) a third timing signal having edge transitions controlled by the second timing signal at times determined by one of the delayed clock signals from the first and second delay lines; and

a controller to change at least one of the first and second amounts of time in the delay lines, to adjust a position of at least one of the first and second edges of the third timing signal.

42. (Currently Amended) A signal processor, comprising:

a first circuit to receive a first timing signal and to generate a second timing signal having edge transitions controlled by the first timing signal at times determined by a logical combination of first and second delayed clock signals, and

a second circuit to generate a third timing signal having edge transitions controlled by the second timing signal at times determined by one of the first and second delayed clock signals, wherein the first timing signal has a period which is a number of times longer than the clock signal.

43. (Canceled)

44. (Previously Presented) The signal processor of claim 42, wherein the first circuit controls the edge transitions of the second timing signal at times when the first and second delayed clock signals have a same logical value.

45. (Currently Amended) A [[The]] signal processor of claim 42, comprising:
a first circuit to receive a first timing signal and to generate a second timing signal having edge transitions controlled by the first timing signal at times determined by a logical combination of first and second delayed clock signals, and
a second circuit to generate a third timing signal having edge transitions controlled by the second timing signal at times determined by one of the first and second delayed clock signals, wherein the second timing signal determines which one of the delayed clock signals controls when the second circuit sets an edge transition of the third timing signal.

46. (Currently Amended) A method, comprising:
generating a second timing signal having edge transitions controlled by a first timing signal at times determined by a logical combination of first and second delayed clock signals; and
generating a third timing signal having edge transitions controlled by the second timing signal at times determined by one of the first and second delayed clock signals, wherein the first timing signal has a period which is a number of times longer than the clock signal.

47. (Canceled)

48. (Currently Amended) A ~~[[The]]~~ method ~~of claim 46~~, comprising:
generating a second timing signal having edge transitions controlled by a first
timing signal at times determined by a logical combination of first and second delayed clock
signals; and
generating a third timing signal having edge transitions controlled by the second
timing signal at times determined by one of the first and second delayed clock signals, wherein
the edge transitions of the second timing signal are controlled at times when the first and second
delayed clock signals have a same logical value.

49. (Currently Amended) A ~~[[The]]~~ method ~~of claim 46~~, comprising:
generating a second timing signal having edge transitions controlled by a first
timing signal at times determined by a logical combination of first and second delayed clock
signals; and
generating a third timing signal having edge transitions controlled by the second
timing signal at times determined by one of the first and second delayed clock signals, wherein
the second timing signal determines which one of the delayed clock signals controls when the
second circuit sets an edge transition of the third timing signal.

50. (Currently Amended) A system, comprising:
a first circuit; and
a second circuit coupled to the first circuit, the second circuit comprising:
a) a first delay line to delay a clock signal by a first amount of time;
b) a second delay line to delay the clock signal by a second amount of time;

- c) a signal processor to generate:
 - a first timing signal from the clock signal,
 - a second timing signal having edge transitions controlled by the first timing signal at times determined by a logical combination of the delayed clock signals from the first and second delay lines, and
 - a third timing signal having edge transitions controlled by the second timing signal at times determined by one of the delayed clock signals from the first and second delay lines, wherein the timing signal controls operation of the first circuit, wherein the first timing signal has a period which is a number of times longer than the clock signal

51. (Currently Amended) The system of claim 50 [[28]], wherein the first circuit is one of a processor, power supply, graphical interface, chipset, memory, and network interface.